

FIG. 1

200

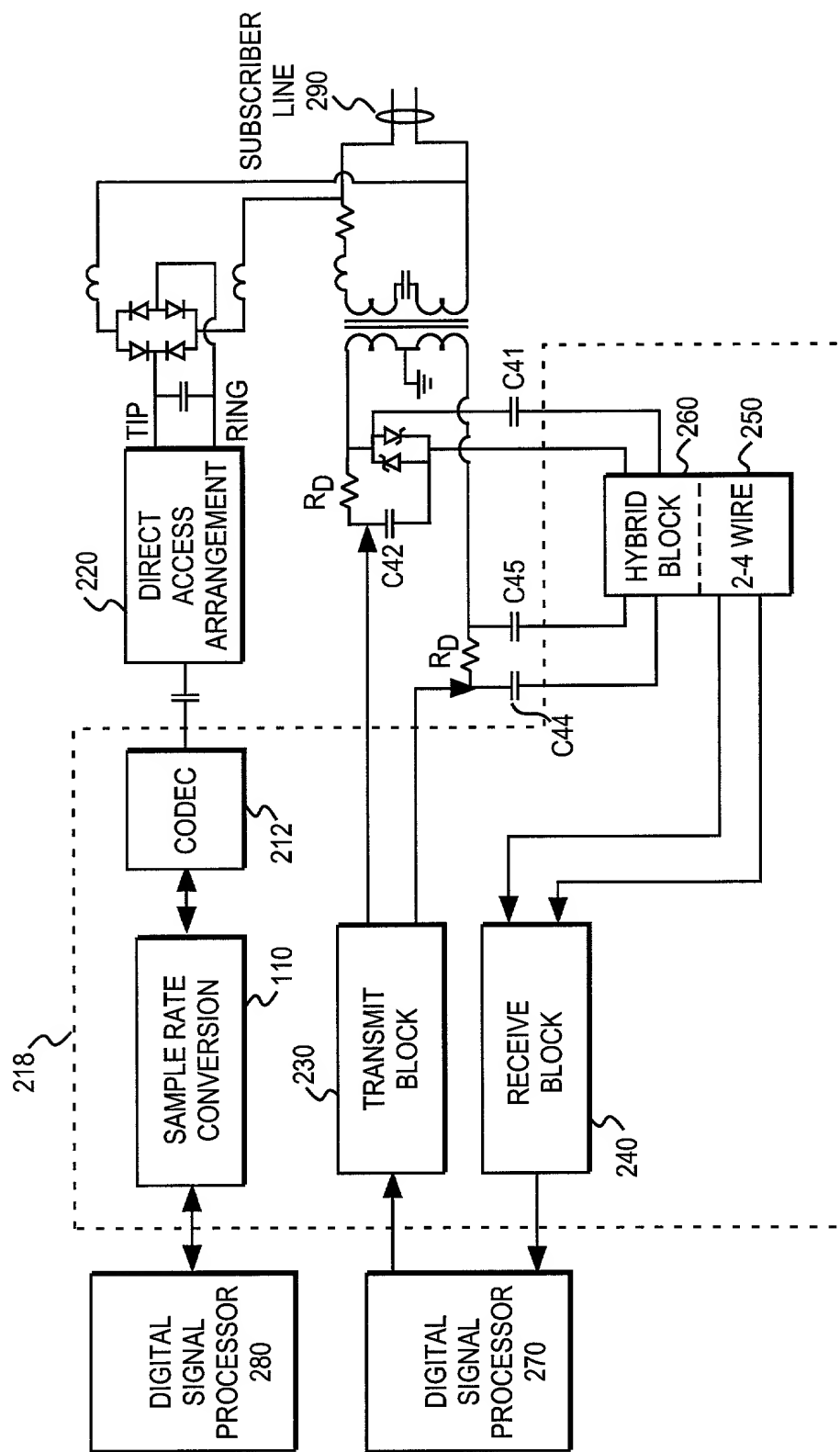
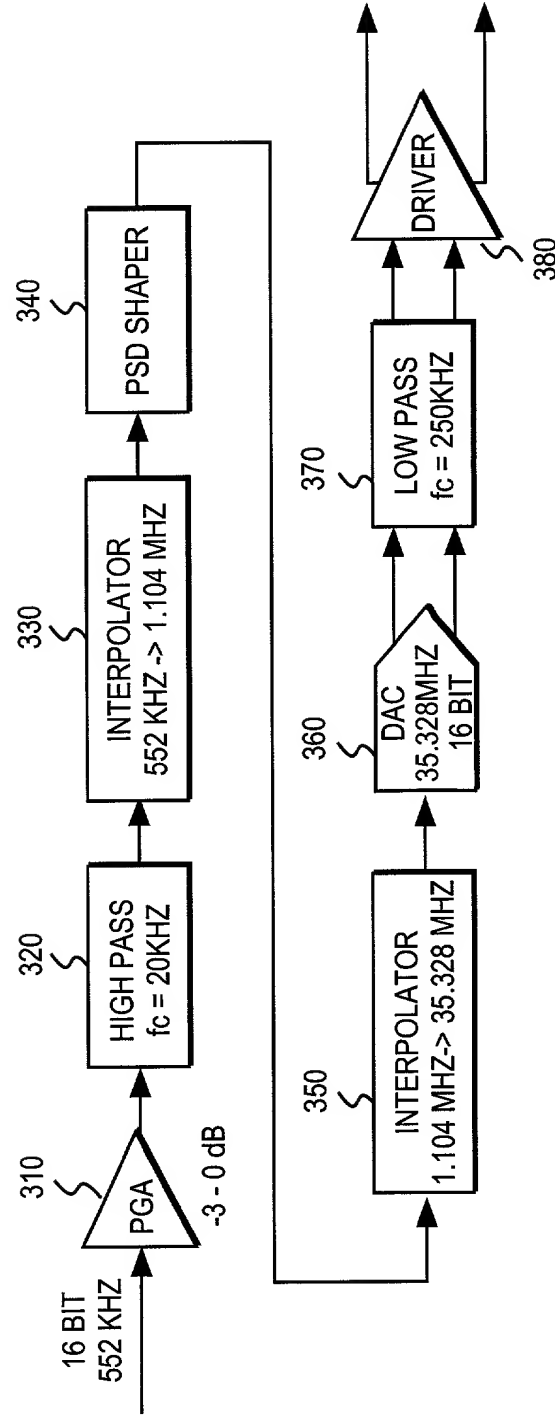


FIG. 2



3
F/G.

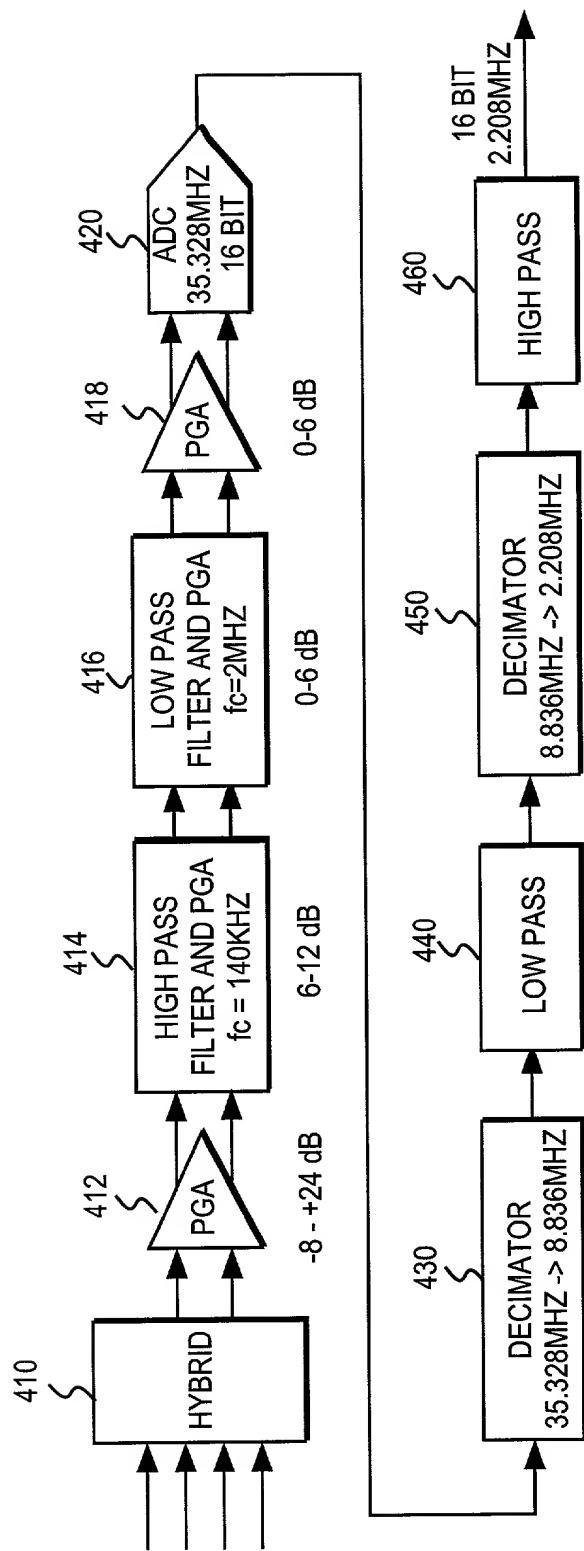


FIG. 4

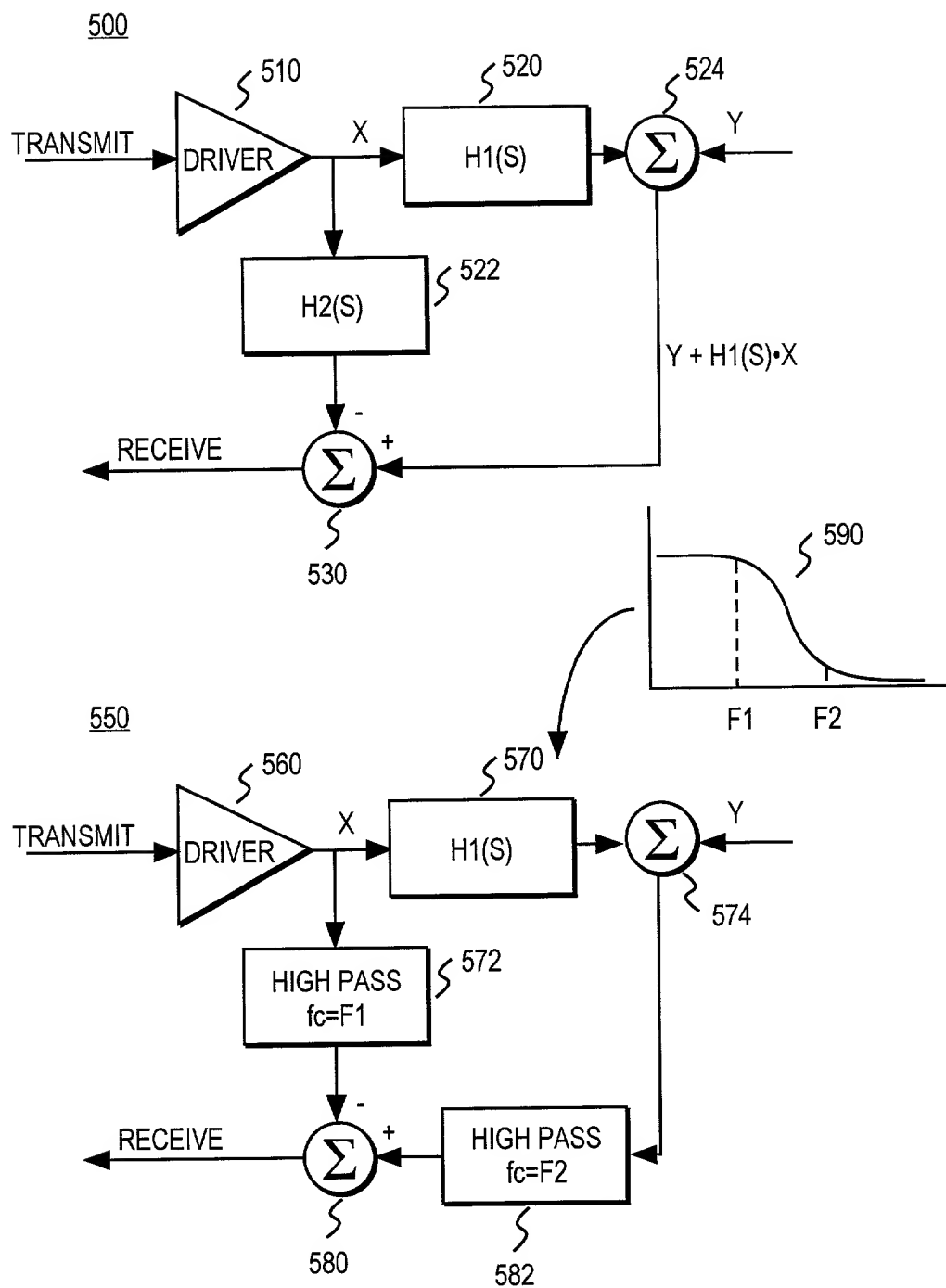


FIG. 5

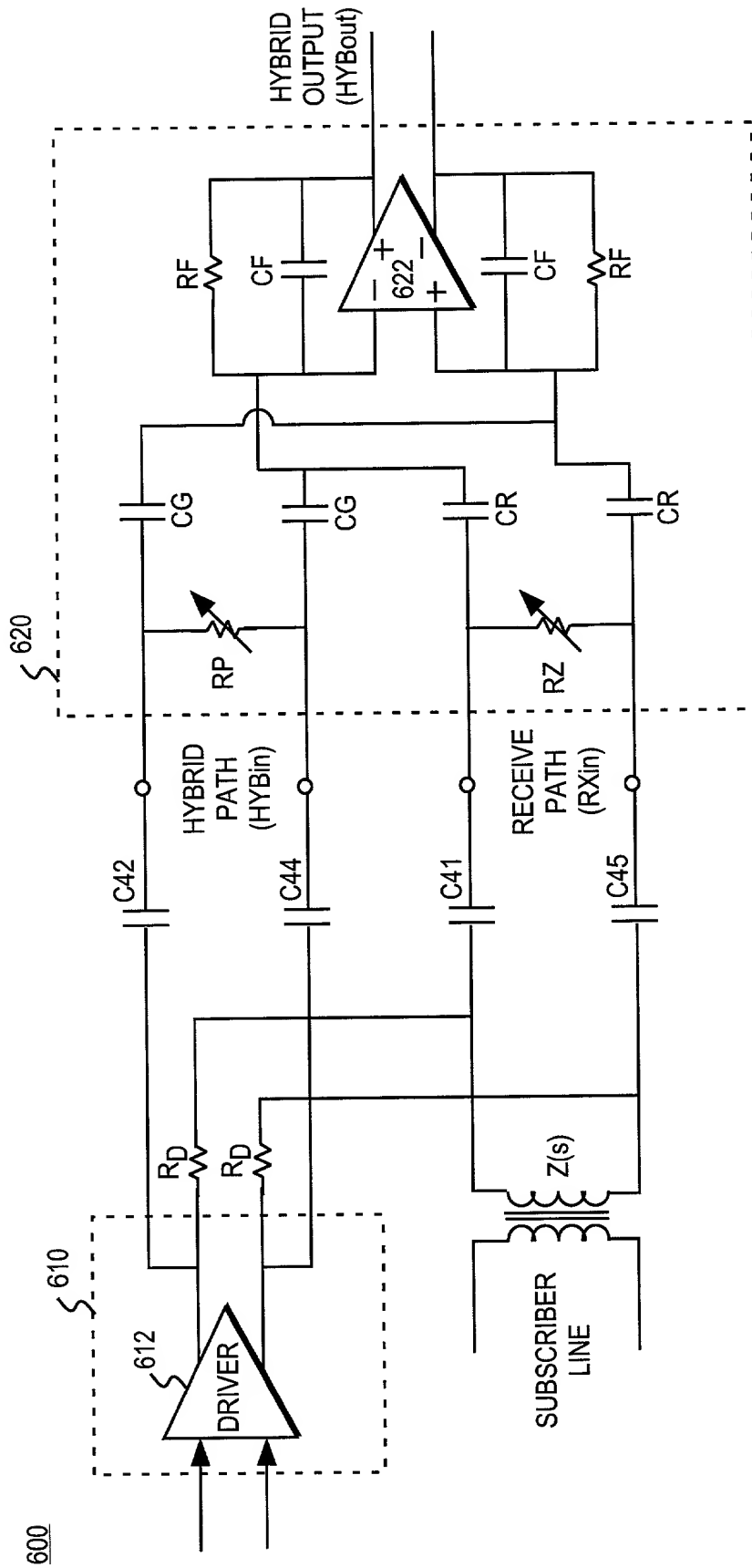


FIG. 6

700

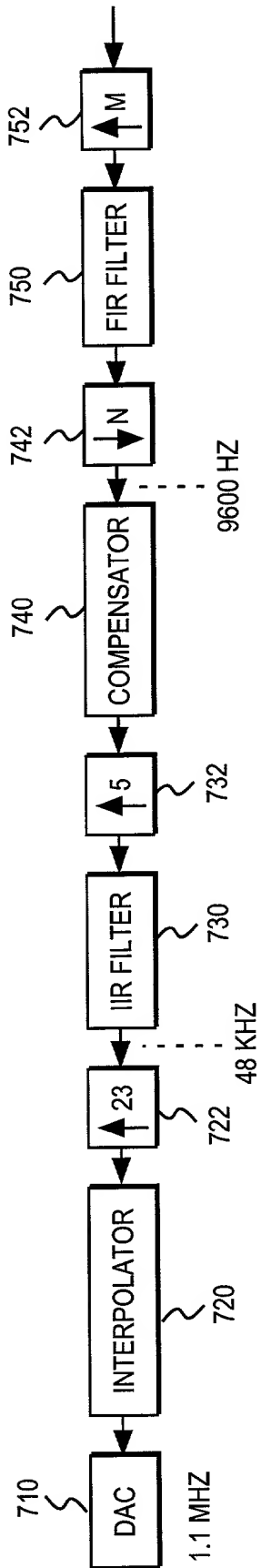


FIG. 7

FIG. 8 is a block diagram of a digital signal processing system. The system includes an ADC (810) receiving a 1.1 MHz input signal. The output of the ADC is fed into a DECIMATOR (820). The output of the decimator is fed into a block labeled 822, which is followed by a block labeled 830 (x26). The output of block 830 is fed into an IIR FILTER (840). The output of the IIR filter is fed into a block labeled 842 (5), which is followed by a block labeled 844 (N). The output of block 844 is fed into an FIR FILTER (850). The output of the FIR filter is fed into a block labeled 860 (M), which produces the final output signal.

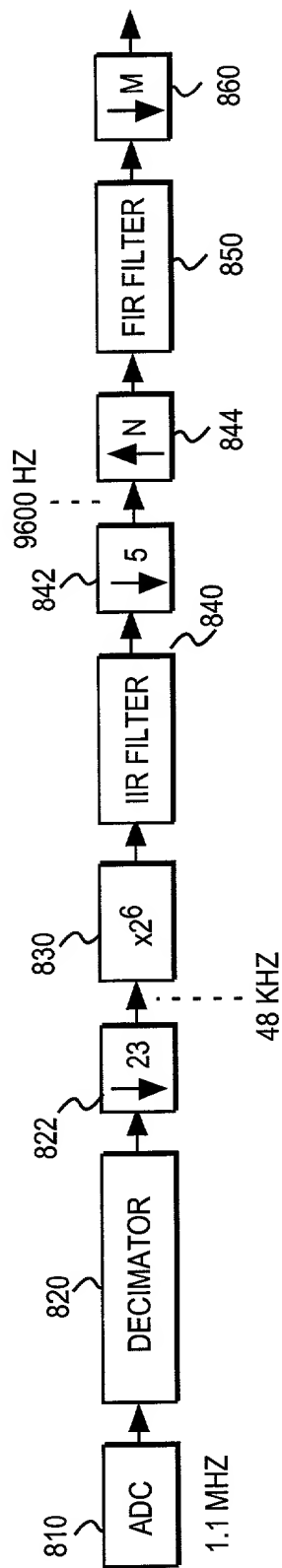


FIG. 8

900

A->D

D->A

f_i	M/N	OPT M/N	f_{audio}	N/M	N/M• f_{audio}
7200	8/6	16/12	9600	12/16	7200
8000	6/5	6/5	9600	5/6	8000
8229	7/6	14/12	9600	12/14	8228.57
8400	8/7	16/14	9600	14/16	8400
9000	16/15	16/15	9000	15/16	9000
9600	1/1	16/16	9600	16/16	9600
10,286	14/15	14/15	9600	15/14	10,285.71

FIG. 9

FIG. 10 is a block diagram of a digital filter structure. The diagram shows a sequence of input data being processed by a series of multipliers (represented by squares) and accumulators (represented by circles labeled B0 through B12). The input data is shifted N places before each computation. The output of the final accumulator is labeled 1020. The diagram is divided into two sections, each of length M, by a vertical line. The first section is labeled 'EVERY Mth COEFFICIENT USED TO CALCULATE NEW VALUE' and the second section is labeled 'INPUT DATA SHIFTS N PLACES BEFORE NEXT COMPUTATION'.

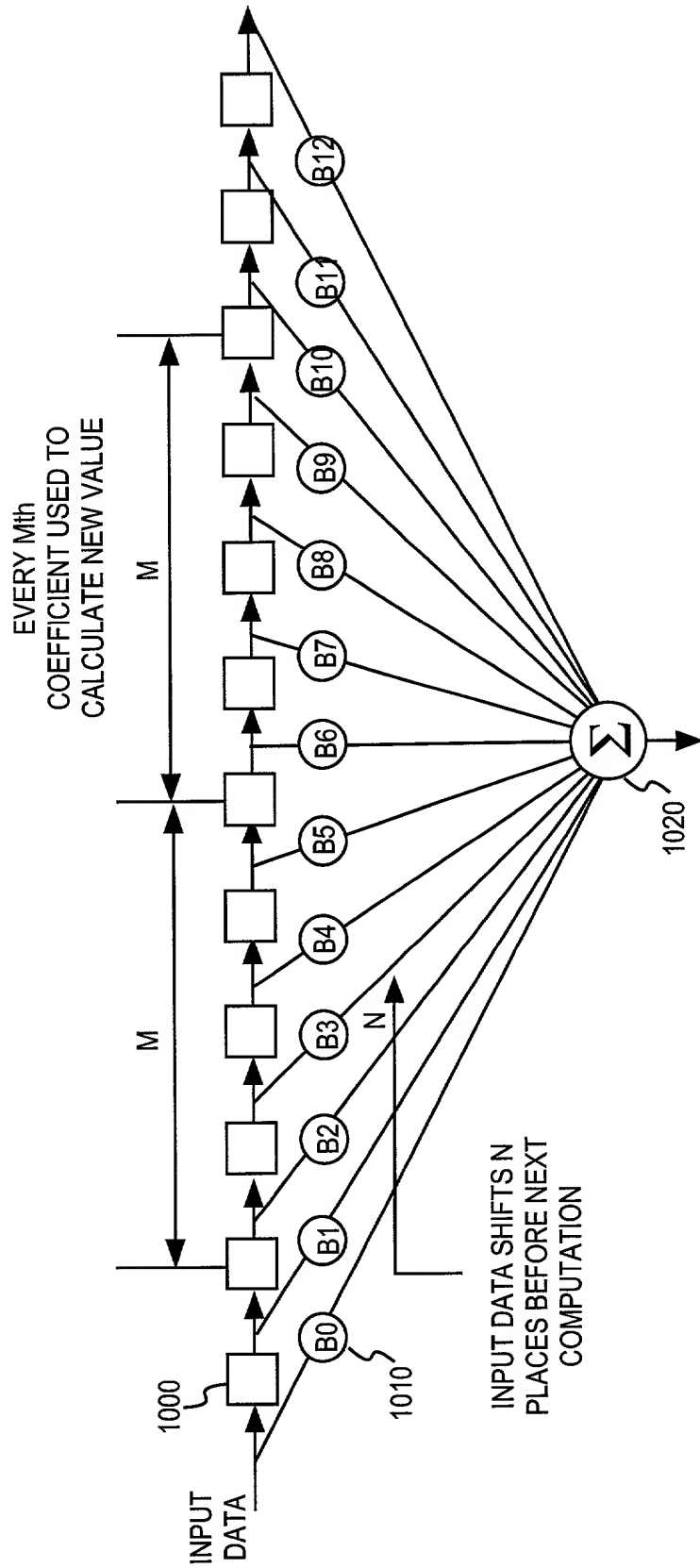


FIG. 10

1100

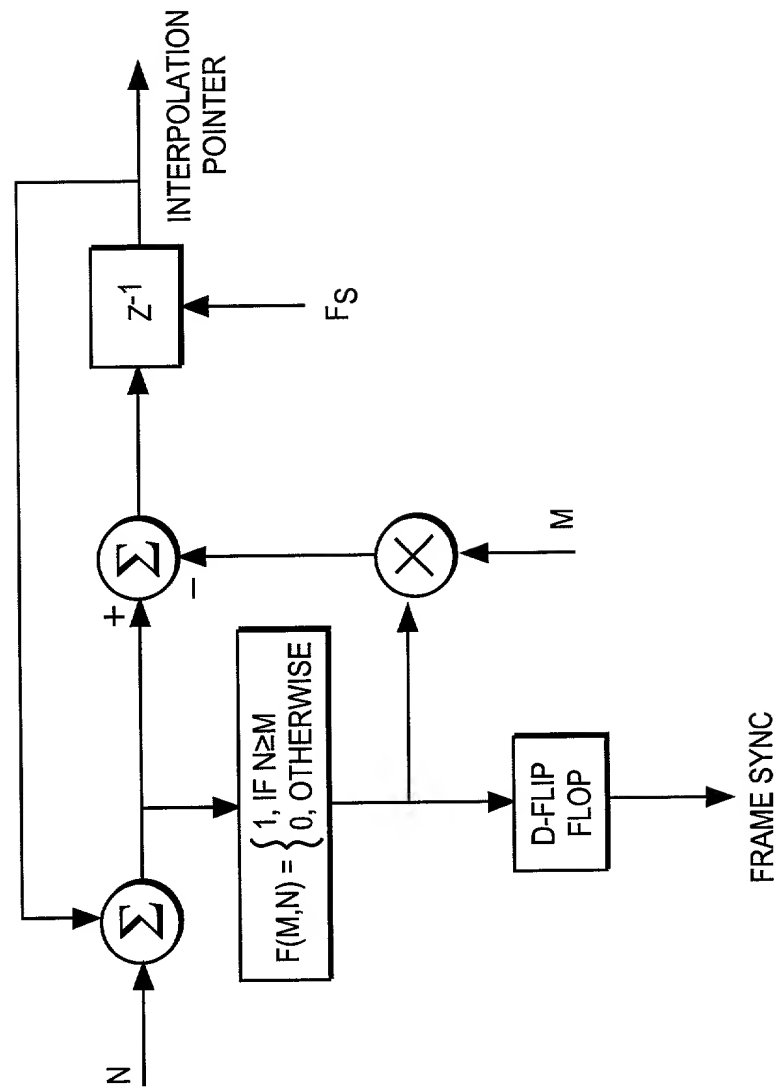


FIG. 11

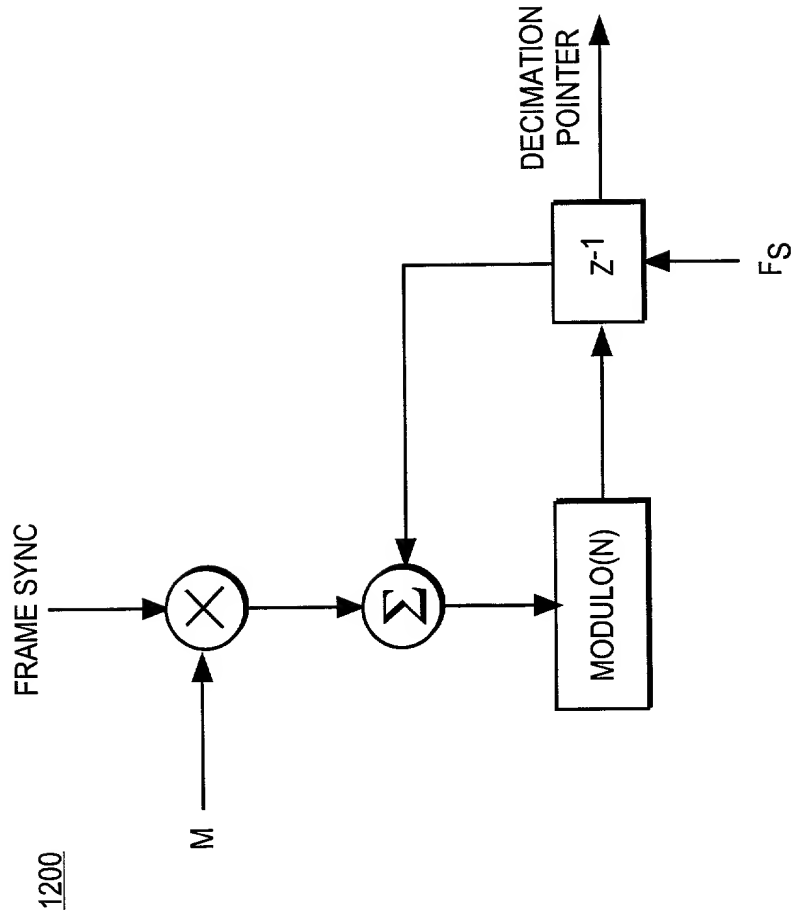


FIG. 12